MGA-62563

Avago Technologies MGA-62563 Current-Adjustable Low Noise Amplifier

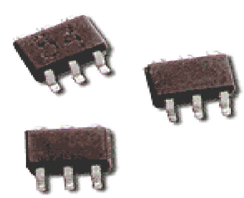
Description

This E-pHEMT RFIC is an easy-to-use high linearity low noise amplifier built-in with Smart Bias function. For Smart Bias function, one external resistor is used to set the bias current taken by the device over a wide range. This allows the designer to use the same part in several circuit positions and tailor the linearity performance and current consumption to suit each position.

It is ideal as an IF amplifier or driver amplifier for Cellular/PCS/W-CDMA base stations, WLL, Fixed Wireless Access, Wireless LAN and other high performance applications in the 0.1 to 3 GHz frequency range.

Lead (PB) Free
RoHS 6 fully compliant

Lifecycle status: Active



Features

Typical performance at 500 MHz 3V/55mA is NF=1.1dB, OIP3=32.5dBm, P1dB=17.4dBm and Ga=22dB

MGA-62563

Current-Adjustable, Low Noise Amplifier

Data Sheet

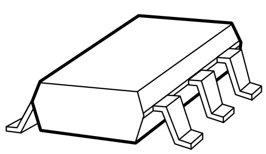
Description

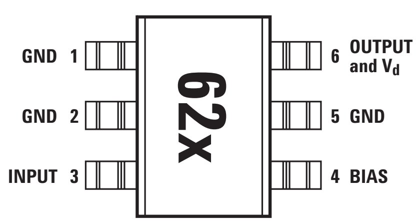
Avago's MGA-62563 is an economical, easy-to-use GaAs MMIC amplifier that offers excellent linearity and low noise figure for applications from 0.1 to 3 GHz. Packaged in an miniature SOT-363 package, it requires half the board space of a SOT-143 package.

One external resistor is used to set the bias current taken by the device over a wide range. This allows the designer to use the same part in several circuit positions and tailor the linearity performance (and current consumption) to suit each position.

The output of the amplifier is matched to 50Ω (below 2:1 VSWR) across the entire bandwidth and only requires minimum input matching. The amplifier allows a wide dynamic range by offering a 0.9 dB NF coupled with a +32.9 dBm Output IP3. The circuit uses state-of-the-art E-pHEMT technology with proven reliability. On-chip bias circuitry allows operation from a single +3V power supply, while internal feedback ensures stability (K>1) over all frequencies.

Pin Connections and Package Marking





Note:
Package marking provides orientation and identification:

"62" = Device Code

"x" = Date code indicates the month of manufacture.

Features

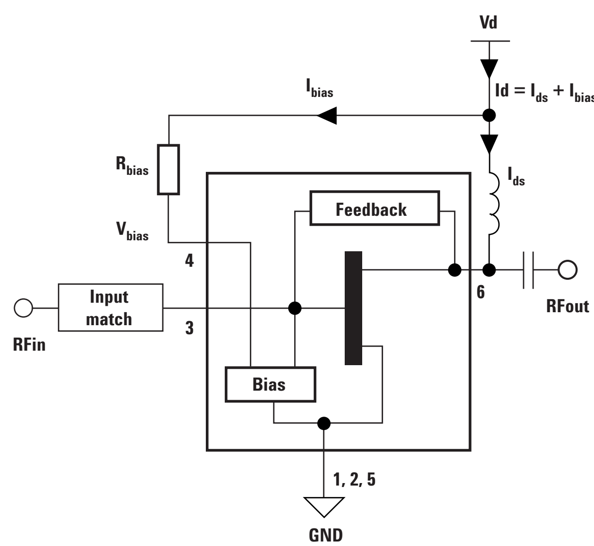
- Single +3V supply
- High linearity
- Low noise figure
- Miniature package
- Unconditionally stable

Specifications

at 500 MHz; 3V, 60 mA (Typ.)

- 0.9 dB noise figure
- 32.9 dBm OIP3
- 22 dB gain
- 17.8 dBm P_{1dB}

Simplified Schematic



MGA-62563 Absolute Maximum Ratings[1]

Symbol	Parameter	Units	Absolute Maximum
V_d	Device Voltage (pin 6)[2]	V	6
I_d	Device Current (pin 6)[2]	mA	100
P_{in}	CW RF Input Power (pin 3)[3]	dBm	21
I_{ref}	Bias Reference Current (pin 4)	mA	12
P_{diss}	Total Power Dissipation[4]	mW	600
T_{CH}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	150
θ_{ch_b}	Thermal Resistance[5]	°C/W	97

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Bias is assumed at DC quiescent conditions.
3. With the DC (typical bias) and RF applied to the device at board temperature T_B = 25°C.
4. Total dissipation power is referred to board (package belly) temperature T_B = 85°C, P_{diss} is required to derate at 10 mW/°C for T_B > 85°C.
5. Thermal resistance measured using 150°C Liquid Crystal Measurement method.

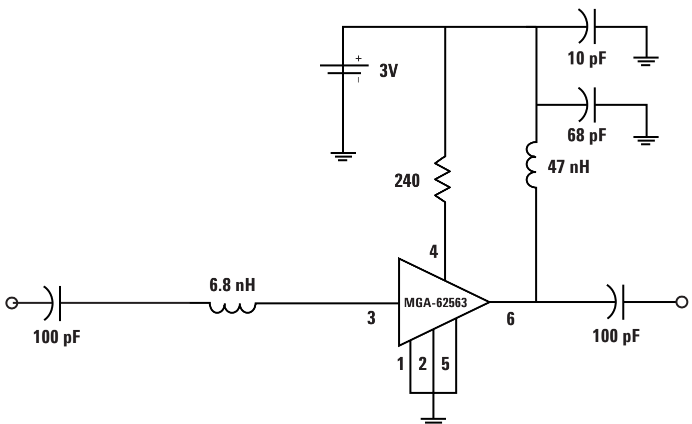


Figure 1. Test circuit of the 0.5 GHz production test board used for NF, Gain and OIP3 measurements. This circuit achieves a trade-off between optimal NF, Gain, OIP3 and input return loss. Circuit losses have been de-embedded from actual measurements.

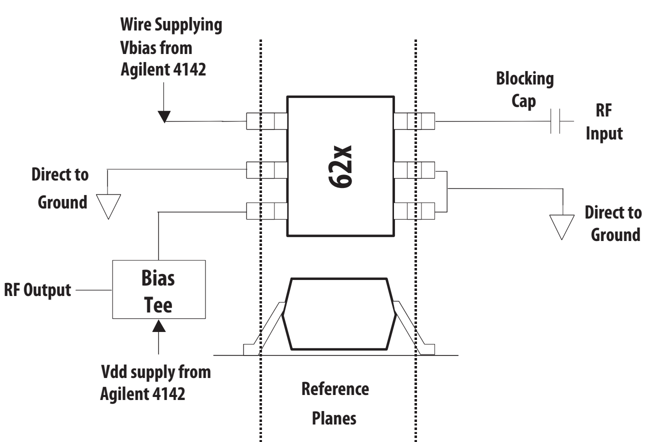


Figure 1b. A diagram showing the connection to the DUT during an S and Noise parameter measurement using an automated tuner system.

MGA-62563 Electrical Specifications

T_C = 25°C, Z_O = 50Ω, V_d = 3V (unless otherwise specified)

Symbol	Parameters and Test Conditions	Freq	Units	Min.	Typ.	Max.	Std Dev
Id [1,2]	Device Current		mA	47	62	77	2.09
NF_{test} [1,2]	Noise Figure in test circuit [1]	f = 0.5 GHz	dB		0.93	1.4	0.06
G_{test} [1,2]	Associated Gain in test circuit[1]	f = 0.5 GHz	dB	20.4	22	23.4	0.36
$OIP3_{test}$ [1,2]	Ouput 3rd Order Intercept in test circuit[1]	f = 0.5 GHz	dBm	30	32.9		0.51
$NF_{50ý}$[3]	Noise Figure in 50Ω system	f = 0.1 GHz	dB		1.1		
		f = 0.2 GHz			1.0		
		f = 0.5 GHz			0.8		
		f = 1.0 GHz			0.9		0.06
		f = 1.5 GHz			1.0		
		f = 2.0 GHz			1.2		
		f = 2.5 GHz			1.3		
		f = 3.0 GHz			1.5		
$\|S_{21}\|^2{}_{50ý}$ [3]	Associated Gain in 50Ω system	f = 0.1 GHz	dB		23.5		
		f = 0.2 GHz			23		
		f = 0.5 GHz			22		
		f = 1.0 GHz			20		0.36
		f = 1.5 GHz			17		
		f = 2.0 GHz			15.5		
		f = 2.5 GHz			14		
		f = 3.0 GHz			13		
$OIP3_{50ý}$[3]	Output 3rd Order Intercept Point in 50Ω system	f = 0.1 GHz	dBm		34.7		
		f = 0.2 GHz			34.7		
		f = 0.5 GHz			34.8		
		f = 1.0 GHz			33.5		0.51
		f = 1.5 GHz			33		
		f = 2.0 GHz			32.3		
		f = 2.5 GHz			32		
		f = 3.0 GHz			31		
$P1dB_{50ý}$[3]	Output Power at 1dB Gain Compression in 50Ω system		f = 0.1 GHz		dBm		18
		f = 0.2 GHz			18		
		f =0.5 GHz			18		
		f = 1.0 GHz			17.6		
		f = 1.5 GHz			17.6		
		f = 2.0 GHz			17.7		
		f = 2.5 GHz			17.9		
		f = 3.0 GHz			17.7		

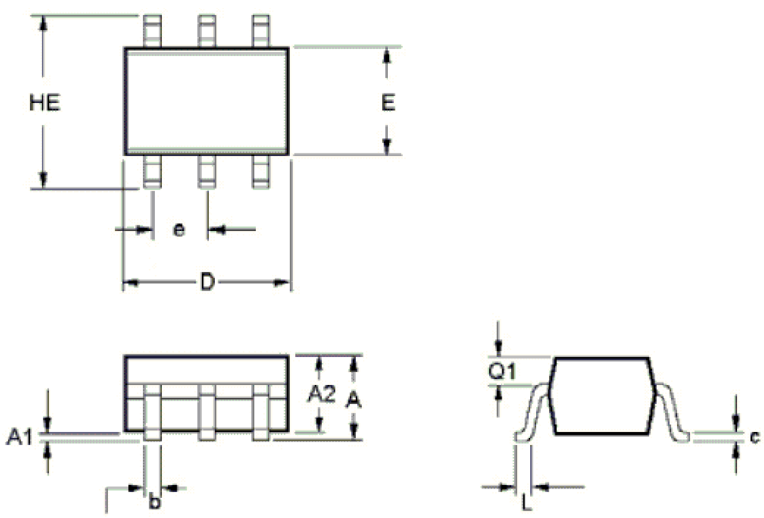
Notes:

1. Guaranteed specifications are 100% tested in the production test circuit as shown in Figure 1, the typical value is based on measurement of at least 500 parts from three non-consecutive wafer lots during initial characterization of this product.
2. Circuit achieved a trade-off between optimal NF, Gain, OIP3 and input return loss.
3. Parameter quoted at 50Ω is based on measurement of selected typical parts tested on a 50Ω input and output test fixture.

Ordering Information

Part Number	No. of Devices	Container
MGA-62563-TR1G	3000	7" Reel
MGA-62563-TR2G	10000	13"Reel
MGA-62563-BLKG	100	antistatic bag

SOT-363/SC-70 (JEDEC DFP-N) Package Dimensions



Symbol	Dimensions Min (mm)	Max (mm)
E	1.15	1.35
D	1.80	2.25
HE	1.80	2.40
A	0.80	1.10
A2	0.80	1.00
A1	0.03	0.10
e	0.650 BCS	0.650 BCS
b	0.15	0.30
c	0.10	0.20
L	0.10	0.30